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APPLICATION NO.	1	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,535		01/18/2002	Hussein S. El-Ghoroury	5444P006	9292
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
055	10/051,535	EL-GHOROURY, HUSSEIN S.				
Office Action Summary	Examiner	Art Unit				
	Jason Mitchell	2193				
The MAILING DATE of this communication apporteriod for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filled after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 27 De	ecember 2005					
	action is non-final.	•				
<u>'</u>	<u></u>					
closed in accordance with the practice under E.	·					
Disposition of Claims						
·						
4) Claim(s) 1-18,20 and 21 is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5)		·				
<u> </u>	election requirement	·				
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9) The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
Applicant may not request that any objection to the o	drawing(s) be held in abeyance. See	37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119		·				
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents	have been received.	·				
2. Certified copies of the priority documents		on No.				
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)				
2) Delice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	te				
) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) 6) Other:						
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DETAILED ACTION

This application claims priority to U.S. provisional applications 60/262803 and 60/268835 and 60/268836 filed on 1/19/01, 2/13/01 and 2/13/01, respectively. This action is in response to remarks filed on 12/27/05

At Applicant's request, claims 1-8, 12 and 16-17 have been amended, claim 19 has been canceled and claims 20 and 21 have been added. Claims 1-18 and 20-21 are pending in this case.

Response to Arguments

Applicant's amendments to the specification are appreciated, and go a long way to correcting the issues which caused the objection. However, Examiner has noted that references to "CVM 215" have been replaced with references to "CVM 125". Item 125 of the figure represents a "Temporal" object, and Item 115 represents a "CVM" object. Thus it would appear the reference to "CVM 125" is incorrect, and the objection will be maintained.

Applicant's amendments to claims 16 and 17 are sufficient to overcome the objections to those claims, which are consequently withdrawn.

Applicant's amendment to claim 12 is sufficient to overcome the 35 USC 112 2nd rejection to that claim, which is consequently withdrawn.

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Applicant's amendments to claims 1-8 are sufficient to overcome the 35 USC 101 rejections to those claims, which are consequently withdrawn.

Applicant's arguments on pp. 12-14 regarding the rejection of claims 1-18 have been fully considered but are not persuasive.

In the last full paragraph on pg. 13, Applicant states:

<u>El-Ghoroury</u> does not disclose the forgoing features of the Applicant's invention, particularly in regards to use of *design vectors* to decompose the matched instruction set processor system into and to analyze and map the interconnected *design vectors* into specific hardware and software elements. <u>El-Ghoroury</u> discloses an application specific processor design method based on using a library of predesigned function blocks. <u>El-Ghoroury</u> as a whole is silent as to the use of design vectors to decompose the matched instruction set processor system into and to analyze and map the interconnected design vectors into specific hardware and software elements, as in the Applicant's invention.

Examiner respectfully disagrees. First, the passage cited by Applicant (starting at pg. 7 line 7) does not discuss "design vectors" but instead refers to "vectors", "functional vectors" and "interconnect vectors" and thus can not be construed as an "explicit definition" of the term, as would be required to incorporate such limitations into the claims.

Further, pg. 7, lines 13-14 of Applicant's specification disclose, "Vectors are the most basic building blocks with which the terminal architectural model can be constructed." Examiner does not recognize a patentable distinction between such "vectors" and El-Ghoroury's disclosure of "fundamental application specific processes" (col. 9, lines 34-38). Nor does Applicant appear to present an indication of functional differences between the two.

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Additionally, it is Examiner's understanding that El-Ghoroury's use of "a library of predesigned function blocks" (col. 9, lines 39-41) represents an aspect of "analyzing and mapping the interconnected design vectors into specific hardware and software elements", as required by the claims.

Thus, the rejection of claims 1-18, are maintained.

The Abandonment of 10/052,312 application overcomes the Double Patenting rejection made in view of that application, which is consequently withdrawn. However revival of the 10/052,312 would require reinstatement of this rejection.

Further, it is noted that the 10/051,217 application has also been abandoned, and the corresponding rejections are withdrawn.

It is noted that a properly filed Terminal Disclaimer with respect to the 10/156,170 application would overcome the corresponding Double Patenting rejections. However, the mere offer to file a Terminal Disclaimer does not.

Specification

The disclosure is objected to because of the following informalities: Many references to the drawings are miss-labeled. For example on pg. 13 of the amended specification, references to the CVM of Fig. 3A use the reference number 125, while the drawing is labeled with 115. Applicant's cooperation is requested in detecting and correcting any errors of this nature of which applicant may become aware.

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Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,867,400 to El-Ghoroury et al. (El-Ghoroury).

Regarding Claims 1, 9: El-Ghoroury discloses a method to efficiently design and implement a matched instruction set processor system, including: analyzing and mapping design specifications of the matched instruction set processor into application components (col. 3, lines 47-51 'analyzes the design requirements ... and describes them in terms of a subset of application specific function blocks'), each application component representing a reusable function commonly used in digital communication systems (col. 3, lines 47-51 'application specific function blocks selected from the library'); decomposing the matched instruction set processor system into interconnected design vectors (col. 9, lines 34-37 'decomposed into fundamental application specific processes'), and analyzing and mapping the interconnected design vectors into specific hardware and software elements (col. 10, lines 1-2 'the design is released for ASIC layout and fabrication').

Regarding Claims 2, 10: The rejections of claims 1 and 9 are incorporated, respectively; further El-Ghoroury discloses performing a behavioral analysis of the matched instruction set processor system to ensure compliance with the design

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specifications (col. 9, lines 52-54 'ascertain whether the ... interfaces are compliant with the design specifications').

Regarding Claims 3, 11, 12: The rejections of claims 1, 9 and 9 are incorporated, respectively; further El-Ghoroury discloses performing a requirement analysis of the design specifications of the matched instruction set processor system to generate a behavioral model (col. 9, lines 52-54 'Behavioral level simulation is performed'); and representing the behavioral model using application components (col. 3, lines 47-51 'application specific function blocks selected from the library').

Regarding Claims 4, 13: The rejection of claims 1 and 9 are incorporated, respectively; further El-Ghoroury discloses mapping the application components into corresponding architectural components (col. 9, line 67-col. 10, line 2 'the design is released for ASIC layout and fabrication').

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,867,400 to El-Ghoroury et al. (El-Ghoroury) in view of US 6,484,304 to Ussery et al. (Ussery).

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Regarding Claims 5, 14: The rejections of claims 4 and 13 are incorporated.

respectively; further El-Ghoroury does not explicitly disclose decomposing each

application component into processing pipelines to satisfy system processing and timing

requirements.

Ussery discloses decomposing each application component into processing pipelines to

satisfy system processing and timing requirements (col. 6, lines 48-54 'partitioned into

microtasks taking into consideration ... opportunities for software pipelining').

Regarding Claims 6, 15: The rejections of claims 5 and 14 are incorporated,

respectively; further El-Ghoroury does not explicitly disclose decomposing each

processing pipeline into design vectors, including functional design vectors and

interconnect design vectors.

Ussery discloses decomposing each processing pipeline into design vectors, including

functional design vectors and interconnect design vectors (col. 6, lines 41-47

'decompose tasks into threads then through dataflow analysis, decompose the threads

into microtasks').

Regarding Claims 7, 16, 17: The rejections of claims 6, 15 and 15 are incorporated,

respectively; further El-Ghoroury does not explicitly disclose using the functional design

vectors to represent design information for at least one functional aspect of the

processing pipeline, and using the interconnect design vectors to contain connectivity

characteristics of the processing pipeline.

Ussery discloses using the functional design vectors to represent design information for

at lease one functional aspect of the processing pipeline (col. 5, lines 2-4 'Each

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microtask is a ... program for a target task engine'); and using the interconnect design vectors to contain connectivity characteristics of the processing pipeline (col. 6, lines 49-52 'partitioned into microtasks taking into consideration ... flow of control').

Regarding Claims 8, 18: The rejections of claims 7 and 17 are incorporated, respectively; further El-Ghoroury discloses decomposing the matched instruction set processor system into interconnected design vectors further includes: providing in each design vector, a run method (col. 3, lines 4-6 'engines that executes microtask instructions'), a conjugate virtual machine (col. 6, lines 64-67 'A microtask analyzer and code generator'), and an invocation method (col. 3, lines 4-6 'engines that executes microtask instructions') and inherently discloses a binding header method and a binding trailer method (col. 3, lines 28-30 'the compiler may insert direct memory data references in each of the microtasks').

Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,867,400 to El-Ghoroury et al. (El-Ghoroury) in view of Turing Completeness.

Regarding Claim 20-21: The rejections of claims 1 and 9 are incorporated respectively; further, El-Ghoroury does not explicitly disclose the use of JAVA to represent his design vectors (col. 9, lines 34-37 'decomposed into fundamental application specific processes'), but does disclose the use of "a high order programming language" (col. 3, lines 65-66).

"Turing completeness is significant in that every plausible design for a computing device so far advanced can be emulated by a universal Turing machine" (see the second

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paragraph of the 'Turing completeness' article) and was first described in 1936 by Alan Turing (see the first paragraph in the 'Turing machine' article). As further indicated in the 'Turing completeness' article "Most programming languages, conventional and unconventional, are Turing-complete" (see the bottom half of pg. 2). Thus it would have been obvious to a person of ordinary skill in the art at the time of the invention that "Java programming language" as claimed, would have been a suitable language with which to implement the "design vectors" and thus would represent an obvious modification to the disclosure of El-Ghoroury. (see MPEP 2144.07)

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer <u>cannot</u> overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1, 9, and 19 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1, 11, and 21, respectively, of copending Application No. 10/156,170 (170). This is a <u>provisional</u> double patenting rejection since the conflicting claims have not in fact been patented.

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Claims 1, 11 and 21 of the 170 reference are identical to 1, 9 and 19, respectively, of the instant application.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Mitchell whose telephone number is (571) 272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Mitchell 3/13/06

> KAKALI CHAKI SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100

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